AMENDMENTS TO THE CLAIMS:

This listing of claims replaces all prior versions of claims in the application.

Listing of Claims

1 - 19. (canceled)

20. (currently amended) A method of fabricating a semiconductor integrated circuit device comprising:

~~(a) providing a semiconductor substrate having a first main surface,~~

~~(b) forming a first insulating film over said first main surface of said semiconductor substrate,~~

~~(c) forming an embedded interconnection slot in said first insulating film over the main surface,~~

~~(d) forming a connecting hole in a bottom surface of said embedded interconnection slot, connected to a lower conducting layer,~~

~~(e) forming a conducting barrier film over a surface region of the first insulating film outside said embedded interconnection slot and said connecting hole and the bottom surface and side surface of said embedded interconnection slot and said connecting hole,~~

~~(f) forming a metal film having copper as its main component over the conducting barrier film so as to fill said embedded interconnection slot and said connecting hole,~~

~~(g) removing the metal film outside said embedded interconnection slot and said connecting hole by a chemical mechanical polishing method using a polishing slurry containing an oxidizing agent of copper and organic acid capable of dissolving an oxide of copper within a corrosion region of copper, thereby forming an~~

~~embedded metal interconnection layer having copper as its main component embedded in said interconnection slot and in said connecting hole in which said conducting barrier film is formed,~~

~~(h) performing plasma treatment to the surface region of the first insulating film and a surface of the embedded metal interconnection layer in a gas atmosphere having reducing properties; and~~

~~(i) after step (h), forming a cap insulating film so as to cover said embedded metal interconnection layer and the upper surface of said first insulating film, wherein:~~

~~the concentration of components other than copper in said embedded metal interconnection layer in the finished semiconductor integrated circuit device does not exceed 0.8At%, and~~

~~the film thickness of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole is less than 10 nm~~

(a) forming a first insulating film over a first major surface of a wafer;

(b) forming a groove in the first insulating film and a hole connected to a bottom surface of the groove in the first insulating film;

(c) forming a barrier metal film over inner surfaces of the groove and the hole, and over an upper surface of the first insulating film;

(d) forming a copper seed layer over the barrier metal layer inside and outside the groove and the hole by copper sputtering with a copper target having a purity of 99.999% or more;

(e) forming a copper film containing copper as its principal component on the copper seed layer inside and outside the groove and the hole by electroplating so as to fill the groove and the hole;

(f) removing the barrier metal film, the copper seed layer, and the copper film formed on the copper seed layer outside the groove and the hole so as to leave a copper interconnection in the groove and the hole, thereby exposing the first insulating film;

(g) performing an ammonia plasma treatment to the exposed surface of the first insulating film and an upper surface of the copper interconnection; and

(h) forming an insulating barrier film on the exposed surface of the first insulating film and the upper surface of the copper interconnection by plasma CVD,

wherein the total concentration of components other than copper in the copper interconnection, when step (h) is completed, does not exceed 0.8At%, and

wherein the film thickness of the thinnest part of the barrier metal film in the groove and the hole is less than 10 nm.

21. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the purity of said copper target is not less than 99.9999%.

22 - 31. (canceled)

32. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the total concentration of components other than copper does not exceed 0.2At%.

33. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the total concentration of components other than copper does not exceed 0.08At%.

34. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the total concentration of components other than copper does not exceed 0.05At%.

35. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein the total concentration of components other than copper does not exceed 0.02At%.

36. (canceled)

37. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein ~~the~~ said film thickness ~~of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole~~ is not more than 5nm.

38. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein ~~the~~ said film thickness ~~of the thinnest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole~~ is not more than 3nm.

39 - 41. (canceled)

42. (currently amended)[[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein ~~the~~ said film thickness ~~of the thickest part of said conducting barrier film in the side walls of said embedded interconnection slot and said connecting hole~~ is not more than 2nm, or there is no ~~conducting~~ metal barrier film.

43. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein ~~the~~ a width of said ~~embedded interconnection slot~~ groove does not exceed 0.4μm.

44. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein ~~the~~ a width of said ~~embedded interconnection slot~~ groove does not exceed 0.25μm.

45. (currently amended) [[A]] The method of fabricating a semiconductor integrated circuit device as defined in Claim 20, wherein ~~the~~ a width of said ~~embedded interconnection slot~~ groove does not exceed 0.2μm.